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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,587	02/21/2001	Dug Jin Park	8733.389.00	8760

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MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
QI, ZHI QIANG	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,587	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-7,9,11,12 and 14-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-7,9,11,12 and 14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 7 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 7 and 16, recitation "developing the negative-type photoresist uses an organic aqueous alkali solution" that is not disclosed in the original specification, and that would constitute as a new matter.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-7, 9, 11-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (AAPA) in view of US 6,022,753 (Park et al) and US 6,077,643 (kumar et al).

Claims 5,14 and 9, 11, 12, AAPA discloses (page 2, line 11 – page 5, line 6; Figs.1A – 1E) that a method of fabricating a liquid crystal display device having a thin film transistor with a gate electrode (13), a gate insulating film (15), an active layer (17), an ohmic contact layer (19), and source electrode (21), drain electrode (22) on a transparent substrate (11) (or forming a thin film transistor having a gate electrode 13, a source electrode 21, and a drain electrode 22 on a transparent substrate 11), and the gate line connected to the gate electrode, the data line (23) connected to the source electrode (21) that define a pixel area, and the method comprising the steps of:

- forming a passivation layer (25) covering the thin film transistor, the gate line and the date line on the transparent substrate (11); and patterning the passivation layer (25) to define a contact hole (26) for exposing the drain electrode (22);
- forming a transparent conductive film (27) being in contact with the drain electrode (22) via the contact hole (26) on the passivation layer (25);
- the exposing step is the ultraviolet ray selectively irradiated onto the photoresist (29) using an exposure mask (31) having a shielding part (32) (opaque part) and a transparent part (33) (page 4, lines 14-20; Figs.1D-1E), i.e., using an exposure mask to expose the photoresist by the light passing through the transparent part of the exposure mask.

AAPA does not expressly disclose that coating a negative-type photoresist on the transparent conductive film and then exposing the negative-type photoresist with an image of pixel electrode, other than a portion corresponding to data line, gate line and

TFT area; and developing the photoresist such that the unexposed area is removed; patterning the transparent conductive film using the photoresist pattern as a mask to form a pixel electrode in contact with the drain electrode via the contact hole; and soft-baked photoresist coating into a thickness of 1-2 μm and at temperature of 100-125°C, and post exposure baking at temperature of 125-145°C; and then removing the photoresist pattern.

However, Park discloses (col.4, line 22 – col. 5, line 30; Figs. 5A – 5D and 6A – 6D) that a manufacturing method of forming a pixel electrode by using a negative photoresist and by a front exposure in which the photoresist (1000) is formed on the transparent conductive layer (ITO) (800), so that the negative photoresist remains when exposed by light, such that the light is irradiated from the front side of the substrate (100) is executed by using a mask having opening pattern over portions of the negative photoresist (1000) on the pixel region (P), and then the exposed portions remains after development, and the ITO layer (800) is etched by using the remaining photoresist as an etch mask to form a pixel electrode (810).

Park also discloses (col.5, lines 31-34) that in the manufacturing method, the pixel electrode (810) overlaps the gate line (200), the gate electrode (210) and data line (600), but the pixel electrode (810) may not overlap them. Therefore, forming an exposed area defining a pixel area also can be other than a portion corresponding to the data line, the gate line and the thin film transistor area, because the fundamental principle is the same as using negative photoresist coating and exposing to light would remove the unexposed portions.

Park indicates (col.5, lines 16-30) that forming the pixel electrode (810) by using the negative photoresist, the pixel defects decreased compared with using a positive photoresist through the front exposure, because if there exist some particles on the unexposed portions of the negative photoresist to light which would cause the adjacent pixel electrodes electrically shorted would be removed (the unexposed portions of the negative photoresist to light is removed).

Park and AAPA do not expressly disclose that the soft-baked photoresist coating into a thickness of 1-2 μm and at temperature of 100-125°C, and post exposure baking at temperature of 125-145°C.

However, Kumar discloses (col.12, lines 65 – 68) that the photoresist composition is softbaked at 120 °C. And the photoresist is a kind of actinic resin, so that coating the photoresist must have a certain thickness and in order to make adhesive the coating that must be hardening and first must be softbaked at a certain temperature, and those skilled in the art would find a proper thickness, such as 1 – 2 μm and a proper softbaking temperature such as 100 – 125°C, and that would have been at least obvious. Kumar discloses (col.11, lines 66-67) that the photoresis coated to an thickness 7320 Å (0.73 μm) that is close to the thickness of 1 μm. Kumar discloses (col.12, line 67 – col.13, line 14) that the resist coating layer after exposure to the light would be post-exposure baked (PEB) at temperature range110 - 140°C to obtain a certain dissolution rate.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to coat a negative-type photoresist on the transparent conductive

film and forming an exposed area defining a pixel area, then exposing the negative-type photoresist with an image of a pixel electrode, then developing the photoresist in which the unexposed area is removed, then patterning the transparent conductive film using the photoresist as a mask to form a pixel electrode in contact with the drain electrode via the contact hole, then remove the photoresist pattern as claimed in claims 5,14, 9, 11 and 12. Since coating a negative-type photoresist and exposing by light and then soft-baking, post baking would harden the coating and obtaining a certain dissolution rate, and that would decrease the adjacent pixel electrodes electrically shorted defects.

Claim 6, Park discloses (col.5, lines 1-15; Fig.6) that the light exposure is executed by using a mask (exposure mask) having opening pattern (the exposure part) over the portions of the negative photoresist (1000) on the pixel region (P) (Fig.6A) (corresponding to the pixel area), so that the shielding part of the exposure mask would corresponding to the data line, gate line and the thin film transistor area (Fig.6A), such that the unexposed portions of the negative photoresist to light would be removed, so as to prevent the adjacent pixel shorting defects.

Therefore, it would have been obvious to those skilled in the art to use the exposure mask as claimed in claim 6 for removing the unexposed portions of the negative photoresist, so as to prevent the adjacent pixel shorting defects.

Claims 7 and 16, AAPA (page 4, lines 21 – 22; Fig.1D-1E) that the photoresist (29) is developed with a developer, such as aqueous alkali solution, and those skilled in the art would find a proper time to obtain a proper developing the photoresist such as 60 – 120 seconds, and that would have been at least obvious. Concerning the

development using an organic alkali aqueous solution that would have been an obvious variation, because the aqueous solution having an inorganic alkali or an organic alkali and both can be used as a developer, and using organic alkali as a developer such as tetramethylamonium hydroxide would prevent the occurrence of staining with an alkali metal, and that using organic alkali did not disclose in the original specification and constitute a new matter.

Claim 15, AAPA discloses (page 5, lines 1-6; Figs.1D-1E) that patterning the transparent conductive film (27) uses a mixed acid as an etchant liquid, and that is using a wet etchant.

Claims 17-18, AAPA discloses (page 4, lines 9-13; Figs.1D-1E) that the passivation layer (25) is patterned to define a control hole (26) so as to expose the drain electrode (22), and the transparent conductive material (ITO) is deposited on the passivation layer (25) so as to electrically contact the drain electrode (22) via the contact hole (26).

Response to Arguments

5. Applicant's arguments filed on Nov.20, 2003 have been fully considered but they are not persuasive.

Applicant's arguments are as follows:

1) None of the references teach the features of the claims, such as coating the photoresist into 1.0 to 2.0 μm, and using soft-bakeing at 100 to 150 °C and post baking at 125 to 145 °C.

2) None of the references teach the features of the claim 7 and 16, such as developing the negative-type photoresist using an organic alkali aqueous solution

Examiner's responses to Applicant's arguments are as follows:

1) Park discloses (col.4, line 22 – col. 5, line 30; Figs. 5A – 5D and 6A – 6D) that a manufacturing method of forming a pixel electrode by using a negative photoresist and by a front exposure in which the photoresist (1000) is formed on the transparent conductive layer (ITO) (800), so that the negative photoresist remains when exposed by light, such that the light is irradiated from the front side of the substrate (100) is executed by using a mask having opening pattern over portions of the negative photoresist (1000) on the pixel region (P), and then the exposed portions remains after development, and the ITO layer (800) is etched by using the remaining photoresist as an etch mask to form a pixel electrode (810).

Kumar discloses (col.12, lines 65 – 68) that the photoresist composition is softbaked at 120 °C. And the photoresist is a kind of actinic resin, so that coating the photoresist must have a certain thickness and in order to make adhesive the coating that must be hardening and first must be softbaked at a certain temperature, and those skilled in the art would find a proper thickness, such as 1 – 2 μm and a proper softbaking temperature such as 100 – 125°C, and that would have been at least obvious. Kumar discloses (col.11, lines 66-67) that the photoresis coated to an thickness 7320 Å (0.73 μm) that is close to the thickness of 1 μm. Kumar also discloses (col.12, line 67 – col.13, line 14) that the resist coating layer after exposure to the light

would be post-exposure baked (PEB) at temperature range110 - 140°C to obtain a certain dissolution rate.

The prior art of record such as US 5,907,008 (Nakano et al) also disclose (col.26, lines 14-19) that the negative type photoresist film (19) is formed to a thickness of 1.0 μm.

Concerning the temperature range and the thickness, according to the MPEP 2144.05, "overlap or lie inside ranges discloses by the prior art" a prima facie case of obviousness exists, and similarly, a prima facie case of obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. The prior art of record such as Kumar and Nakano disclosure establish a prima facie case of obviousness.

2) Concerning the development using an organic alkali aqueous solution that would have been an obvious variation, because the aqueous solution having an inorganic alkali or an organic alkali and both can be used as a developer, and using organic alkali as a developer such as tetramethylamonium hydroxide would prevent the occurrence of staining with an alkali metal, and that using organic alkali did not disclose in the original specification and constitutes a new matter.

The prior art of record such as US 5,476,320 (Taguchi et al), US 6,159,654 (Machida et al) and US 6,187,519 (Sugawara) disclose that an organic alkali used for some negative photoresists as a developer, and Taguchi indicates (col.1, lines 27-38) that using organic alkali aqueous solution as a developer prevents the occurrence of staining with an alkali metal, and that would have been at least obvious.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. According to the MPEP 2144.03 (D), the newly added reference is added only as directly corresponding evidence to support the prior art common knowledge finding, and it does not result in anew issue or constitute a new ground of rejection, the office action may be made final.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mike Qi
February 6,2004

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800